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EXAMINER

BATAILLE, PIERRE MICHE

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 08/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/651,229

Applicant(s)

WARD, WILLIAM P.

Examiner

Pierre-Michel Bataille

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. Claims 1-23 are presented for examination in the application. The preliminary amendment filed May 12, 2000 is noted. The examiner has considered the information disclosure statement submitted on March 12, 2001.

#### *Objection*

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors.

Claim: Claims 20-22, it appears that "a memory controller" should be -- each memory controller -- for consistency.

Drawing: This application has been filed with informal drawings, which have been objected to because of the problems addressed in the Draft-person. Therefore, the drawings are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

#### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-22 are rejected under 35 U.S.C. 102(a)(e) as being anticipated by US 6,076,139 (Welker et al).

As per claim 1, Welker shows a system (as shown in Fig. 1 and 2) comprising: a memory bus (*multi-channel memory interface 106, Fig. 1; synchronous, high speed Rambus channel 202-208, Fig. 2*) [Col. 3, Lines 31-38]; and a plurality of memory controllers (*memory interface control (MIC) blocks 310, Fig. 3*) [Col. 4, Lines 37-39], each memory controller to generate memory requests on the memory bus (*each memory controller running memory cycles from their respective masters*) [Col. 4, Lines 39-49] according to a priority scheme [Col. 4, Lines 51-54; Col. 8, Lines 16-19].

As per claim 3, Welker discloses the system wherein the predetermined priority scheme comprises a request-select priority scheme [*accesses may be completed out of order with a highest priority access* (Col. 5, Lines 26-34) or *read requests may take priority over write*

*requests [Col. 8, Lines 30-35] processor or other master having write highest priority on selected slot or channel (Col. 8, Lines 16-29)].*

As to claim 4, Welker teaches the memory bus comprising a Rambus channel *(system bridge 106 is a multi-channel memory interface 200 which provides multiple Rambus or memory channel 202-208) [Col. 3, Lines 31-39].*

As per claims 6, Welker discloses the system wherein the memory bus comprises plural control portions *(memory interface control blocks 310, Fig. 3) [Col. 4, Lines 37-39]*, each of the control portions associated with corresponding priority scheme *(memory control block 310 running memory cycles from their respective masters or processor assigned a predetermined priority on predetermined channel) [Col. 8, Lines 16-30].*

As per claim 9, Welker discloses the system wherein each of the memory bus comprises plural portions *(memory interface control channel 0-3)*, each portion associated with a set of memory devices *(Rambus dynamic random access memory (RDRAM)) [Fig. 2; Col. 3, Lines 33-40; Col. 4, Lines 55-58; Col. 7, Lines 33-37].*

As per claim 2, Welker teaches the system wherein the predetermined priority scheme comprises a time slot priority scheme *(time slot priority scheme corresponds to the disclosed channel priority scheme, a well known principle of Rambus channel wherein no master can write to a channel until another master write is completed) [Col. 7, Lines 53-57; Col. 5, Lines 26-29].* Welker at least implicitly teaches the claimed time slot priority scheme because of the disclosed interleaved transactions where write cycles to a channel (i.e. 2) is used while a previous write to another channel (i.e. 1) is not yet completed and because a

lock attempt to channel 1 is held or placed in a queue or is assigned a priority timing (slot) until the previous write to the channel (1) is completed [Col. 5, Lines 23-62; Col. 8, Lines 16-30].

As per claim 5, Welker discloses the system wherein each memory controller generates a memory request during a different predetermined time slot (*one snoop request at a time where a central arbiter prioritizes snoop requests*) [Col. 5, Lines 26-34; Col. 8, Lines 58-61].

As per claim 7, Welker discloses the system wherein the time slot priority scheme are staggered [*interleaved transactions are assigned or arranged in round-robin fashion on selected channel select* (Col. 8, Lines 16-29)].

As per claim 8, Welker discloses the system wherein the control portions comprise a row portion and a column portion (*a well known principle of Rambus channel, well known principle of interleaving in Rambus channel, and embedded feature of the memory channel in Welker because row accesses separated from column accesses over separated row access pins and column access control pins would provide interleaved transactions, as Welker's system features interleaved transactions over RAMBUS channel to control performance gained*) [Col. 3, Lines 48-55; Col. 8, Lines 8-30]; Walker's system handles separate row and column accesses simultaneously [Col. 3, Lines 46-55].

As per claim 10, Welker discloses a system (as shown in Fig. 1 and 2) comprising: a memory bus (*multi-channel memory interface 106, Fig. 1; synchronous, high speed Rambus channel 202-208, Fig. 2*) [Col. 3, Lines 31-38]; and a plurality of memory controllers

(*memory interface control (MIC) blocks 310, Fig. 3*) connected to the memory bus [Col. 4, Lines 37-39], each memory controller to monitor memory requests generated by another memory controller (*each MIC controller includes its own snoop controller 706 generating snoop cycles and return snoop transactions response which the requesting controller acknowledges*) [Col. 4, Lines 50-54; Col. 8, Line 58 and Col. 9, Line 20] in performing memory related actions (*snoop accesses, memory read/write, read-modify write*) [Col. 5, Lines 15-45].

As per claims 11, Welker discloses the memory related actions to comprise read-modify-write action [Col. 5, Lines 36-40].

As per claim 12, Welker discloses the memory related actions to comprise a cache coherency action [Col. 5, Lines 26-40].

As per claim 13, Welker discloses the memory related actions to comprise a memory request (memory read and write requests) [Col. 4, Lines 1-4; Col. 5, Lines 20-40; Col. 6, Lines 19-24].

As per claims 14, Welker discloses the memory controller to determine if the memory bus is available based on outstanding requests from other memory controllers (*central snoop arbiter to receive individual snoop requests from each memory channel to determine snoop cycle priority when processor contending for the same channel with another master implementing read and write accesses*) [Col. 2, Line 66 to Col. 3, Line 5; Col. 5, Lines 46-64; Col. 7, Lines 24-26].

As per claim 15, Walker discloses a system (as shown in Fig. 1 and 2) implemented a method providing a plurality of memory controllers (*memory interface control (MIC) blocks 310, Fig. 3*) [Col. 4, Lines 37-39] on a memory bus (*multi-channel memory interface 106, Fig. 1; synchronous, high speed Rambus channel 202-208, Fig. 2*) [Col. 3, Lines 31-38]; the memory controllers generating requests on the memory bus (*each memory controller running memory cycles from their respective masters*) [Col. 4, Lines 39-49]; and each memory controller monitoring memory requests generated by another memory controller (*each MIC controller includes its own snoop controller 706 generating snoop cycles and return snoop transactions response which the requesting controller acknowledges*) [Col. 4, Lines 50-54; Col. 8, Line 58 and Col. 9, Line 20] in performing memory related actions (*snoop accesses, memory read/write, read-modify write*) [Col. 5, Lines 15-45].

As per claim 16, Walker discloses generating the requests comprising generating Rambus command packets (*packet type data received and transmitted from and to Rambus DRAM (RDRAMs) by a transaction protocol according to the Rambus channel*) [Col. 7, Lines 53-63].

As per claims 17, Walker discloses generating the requests comprising the memory controllers generating the requests one at a time according to predetermined priority scheme (*one snoop request at a time where a central arbiter prioritizes snoop requests*) [Col. 5, Lines 26-34; Col. 8, Lines 58-61].

As per claim 18, Welker teaches generating the requests according to a time slot priority scheme (*time slot priority scheme corresponds to the disclosed channel priority scheme, a well known principle of Rambus channel wherein no master can write to a channel until another master write is completed*) [Col. 7, Lines 53-57; Col. 5, Lines 26-29]. Welker at least teaches the



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claimed time slot priority scheme because of the disclosed interleaved transactions where write cycles to a channel (i.e. 2) is used while a previous write to another channel (i.e. 1) is not yet completed and because a lock attempt to channel 1 is held or placed in a queue or is assigned a priority timing (slot) until the previous write to the channel (1) is completed [Col. 5, Lines 23-62; Col. 8, Lines 16-30].

As per claim 19, Welker discloses generating the requests according to a request-select priority scheme [*accesses may be completed out of order with a highest priority access* (Col. 5, Lines 19-34) *and processor or other master having write highest priority on selected channel* (Col. 8, Lines 16-29)].

As per claim 20, Welker discloses each memory controller determining when to generate a memory request based on the monitoring (*receiving snoop requests from a plurality of sources and determining priority among the snoop requests received and granting highest priority to one of the snoop requests*) [Col. 5, Lines 26-29; Col. 8, Lines 58-61].

As per claim 21, Welker discloses each memory controller determining if a lock has been asserted due to the presence of a read-modify-write transaction [Col. 5, Lines 29-40].

As per claims 22, Welker discloses each memory controller (*each memory control block (MIC) comprises page hit detector-controller 712*) performing a cache coherency action based on the monitoring (*snoop action or page hit*) [Col. 7, Line 64 to Col. 8, Line 12; Col. 8, Line 67 to Col. 9, Line 31].

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,076,139 (Welker et al).

As to claims 23, Welker discloses the invention as claimed, monitoring requests from another controller on a memory bus and determining if a memory request can be generated on the memory bus based on the monitoring, as details above with respect to claims 1-22 (see Col. 4, Lines 50-54; Col. 5, Lines 26-29; Col. 8, Lines 58-66); Welker does not specifically disclose an article of manufacture comprising one or more storage media containing instructions when executed to cause the memory controller implement the control functions, as noted above. However, one having ordinary skill in the art would have recognized that it is well known in the art that computer storage medium (i.e. floppy, CD-ROM, etc.) carry computer executable instructions because it would facilitate transporting and installing executable instruction on other systems. For example, a copy of Microsoft Windows Operating system software is carried on a CD-ROM from which Windows operating system can be installed onto other system, which is a lot easier than running a long cable to install the operating system from a network based server. Therefore, it would have been obvious to one having ordinary skill in the

art, to put Welker's control system and method on designed instructions to be carried on a computer storage media, because it would have facilitated the transporting, installing and implementing of Welker's method on other systems.

### **Conclusion**

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

On page 4, The Logical Layer, and 9 of "RAMBUS, Technology Overview" (IDS provided reference), it is quoted that "*On Rambus channel, data and control bits move in packets. Each packet is four cycles in length wherein a totally independent control and address bus is split into two groups of pins, one for row command and the other for column commands and wherein each bus allows a row command, column command and data to be transferred at the same time to different banks of a Rambus dynamic random access memory (RDRAM) or to different RDRAMs.*" This provides evidence that support the assertion above (see claim 8).

"A Memory Controller For Interleaving Over A Single Rambus" (Zacharenia Xanthaki), [www.ics.forth.gr/proj/arch-vlsi/sw\\_arch/interlRambus.ps.gz](http://www.ics.forth.gr/proj/arch-vlsi/sw_arch/interlRambus.ps.gz), features similar to the claimed invention, "*In an interleaved Rambus, a new request can be issued in the middle of some previous transactions. In this case, the controller should know the state of the Rambus Channel, i.e. which time slots are free and which are reserved, as well as the timing requirements of the waiting requests in order to decide whether each of them would cause any conflicts. Since the delays between the request, acknowledge,*

*and data packets are fixed during the system operation, the timing requirements of each request are fully specified.* The reference is also provided evidence to support the assertion above (see claims 2, 5, 7, and 18).

US 6,393,534 (Chen et al) discloses hardware generated control system comprising scheduler for prioritizing requests according to selected priority scheme.

US 6,381,658 (Swaminathan) discloses memory controller scheduling times for packets based upon time constraints over Rambus memory channel.

US 5,894,586 (Marks et al) discloses establishing an order of access to memory by the plurality of processing units by assigning each of the plurality of processing units a time slot in a device access cycle using a micro controller operating with Rambus DRAM.

US 6,026,464 (Cohen) shows a system comprising a memory bus; and a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a priority scheme.

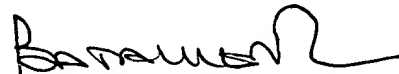
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703)

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746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



Pierre-Michel Bataille  
Examiner  
Art Unit 2186

August 8, 2002